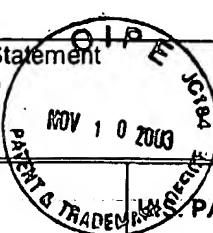



Form PTO-1449 (Modified)		Atty D cket N : P12759C		Serial No.: 10/618,226	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Robert Chau et al.	
				Filing Date: July 11, 2003	



REFERENCE DESIGNATION						
Examiner Initials	Document No.	Document No.	Inventor	Class	Sub-Class	Filing date if appropriate
~	AA	6,121,094	Gardner et al.	438	287	
~	AB	6,436,777	Ota	438	305	
~	AC	6,514,828	Ahn et al.	438	297	
~	AD	6,617,209	Chau et al.	438	240	
~	AE	6,617,210	Chau et al.	438	240	
~	AF	US2002/0197790	Kizilyalli et al.	438	240	
~	AG	US2003/0045080	Visokay et al.	438	591	
	AH					
	AI					
	AJ					
	AK					
	AL					
	AM					
	AN					
	AO					
	AP					

FOREIGN PATENT DOCUMENTS							
No.	Document No.	Date	Country	Class	Sub-Class	Translation	
	AQ						
	AR						
	AS						
	AT						
	AU						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
~	AV	Polishchuk et al., "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion," www.eesc.berkeley.edu , 1 page.
	AW	
	AX	
	AY	
	AZ	

Examiner 	Date Considered 4/15/04
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[illegible][illegible]

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Application Number	Not yet assigned 10/618, 226
Filing Date	Herewith 7/11/03
First Named Inventor:	Robert Chau et al.
Group Art Unit	Not yet assigned 2813
Examiner Name	Not yet assigned TACK CHEN
Attorney Docket Number	042390P12759C

Sheet 1 of 2

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	Not yet assigned 19/618,226
Filing Date	Herewith 7/11/03
First Named Inventor:	Robert Chau et al.
Group Art Unit	Not yet assigned 2813
Examiner Name	Not yet assigned SACK CHEN
Attorney Docket Number	042390P12759C



Sheet

2

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2

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		Douglas Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistor with High-K Gate Dielectrics", IEEE 2001	
		Robert Chau et al., "A 50nm Depleted-Substrate CMOS Transistor (DST), IEEE 2001	

Examiner
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